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D.   Remarks

Objections to the Specification

The Specification has been amended to address objections raised in the Office Action,
5   and to address other typographical errors.

Objections to Drawings

With regard to FIGS. 4A and 4B, the figures are believed to be adequately labeled. FIGS.
4A and 4B label item 402 as "NV MEMORY". The specification refers to item 402 as a "first
10   nonvolatile memory". FIGS. 4A and 4B label item 410 as "PROM". The specification refers to
this item as a PROM:

[A] second nonvolatile memory 410 may be a mask programmable ROM...[1]

15   Therefore, Applicant respectfully requests reconsideration of this ground for objection.

FIG. 4A has been amended to include the reference character 408 referring to the BIST
data.

FIGS. 6A to 6C have been amended to include the label NV ELEMENTS pointing to
item 606.

20

Claim Objections.

Claims 1-9 and 11-16 were objected to for "grammatical informalities". The rejection
appears to object to the use of the word "store". Applicant traverses this objection on the
grounds that "store" is readily understood. In support of the traversal, Applicant submits a
25   section from The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, as Exhibit
A, which provides an entry and definition for "store".

Claim 18 was objected to for grammatical informalities. Applicant respectfully requests
clarification of this ground for objection. Claim 18 is believed to meet all statutory requirements
for patentability as related to form.

30   Claim 16 has been amended as suggested by the Examiner.

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[1] See the Specification, Page 11, Lines 18-19.

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Claim 15 has been amended to include the term "store".

Claim 20 was objected to for grammatical informalities. Applicant respectfully requests clarification of this ground for objection. Claim 20 is believed to meet all statutory requirements for patentability as related to form.

5

<u>Claim Rejections.</u>

Applicant thanks the Examiner for the clear statement for the grounds of rejection.

The rejections of claims 1-10 will first be addressed.

10   <u>Rejection of Claims 1 and 2 Under 35 U.S.C. §103(a), based on U.S. Patent No. 5,991,907 (Stroud et al.) in view of U.S. Patent No. 5,889,701 (Kang et al.), further in view of U.S. Patent No. 5,946,267 (Pathak et al.).</u>

The invention of amended claim 1 is directed to a <u>programmable logic device (PLD) assembly</u> that can include a programmable logic circuit that provides functions according to
15   configuration data, including a self-test function. Also included is at least one nonvolatile store <u>of the PLD assembly</u> coupled to the programmable logic circuit that provides self-test configuration data for the programmable logic circuit and can subsequently store user configuration data.

As is well known, to establish a prima facie case of obviousness, a rejection must meet
20   three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

As noted above, Applicant's claim 1 invention includes at least one nonvolatile store that provides self-test configuration data and can store user configuration data. As originally
25   claimed, and as emphasized by Applicant's amendment, the at least one non-volatile store is part of the same <u>PLD assembly</u> as the programmable logic circuit. The cited combination of references is not believed to not show or suggest such a claim limitation.

The rejection admits that while Stroud et al. shows a test controller that retrieves built-in self-test (BIST) configuration data, the reference is silent as to a store being non-volatile[2].
30   However, Applicant adds that Stroud et al. also fails to show any sort of store that is part of a

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[2] See the Office Action, dated 4/24/03, Page 4, Lines 7-8.

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PLD assembly, as claimed. Further, the teachings of *Stroud et al.* teach away from such a claim limitation.

In *Stroud et al.* BIST configuration data is retrieved from a test controller. The reference describes a test controller as automatic test equipment (ATE), a central processing unit (CPU), or

5   a maintenance processor.[3] Thus, *Stroud et al.* teaches the retrieval of BIST configuration data from an independent piece of equipment separate from the FPGA under test. Consequently, the reference not only does not show Applicant's claim limitation, but teaches away from moving BIST configuration data onto the same assembly as a programmable logic circuit, as set forth in claim 1.

10   Modifying *Stroud et al.* in view of *Kang et al.* does not arrive at Applicant's claim limitations, either. The rejection proposes modifying the FPGA under test in *Stroud et al.*, with an in-system programmable FPGA as set forth in *Kang et al.*[4] This modification appears to add no additional teachings over *Stroud et al.* *Stroud et al.* teaches the testing and programming of an FPGA already installed in a system that can be programmed "in system"[5]. Still further, *Kang*

15   *et al.*, teaches away from Applicant's claim limitations, as self-test data, like *Stroud et al.*, is provided by automatic test equipment:

A standard mainframe tester, an Automated Test Equipment (ATE), is programmed to follow the method of the present invention.[6]

20

Thus, both *Stroud et al.* and *Kang et al.* teach away from Applicant's claim limitations of "at least one store of a PLD assembly that provides self-test configuration data", by having all test data retrieved on separated ATE.

Modifying *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.* still fails

25   to show Applicant's claim 1 limitations. *Pathak et al.* discloses a configuration memory that can initialize a programmable logic device. However, *Pathak et al.* provides no mention of (1) such a configuration memory being part of an assembly that includes a programmable logic circuit or

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[3] See *Stroud et al.*, Col. 4, Lines
[4] See the Office Action, dated 4/24/03, Page 4, "Combination A".
[5] See *Stroud et al.*, Col. 7, Lines 46-52.
[6] *Kang et al.*, Col. 2, Lines 22-23.

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(2) such a memory storing <u>self-test</u> data for the programmable logic circuit. Accordingly, the reference cannot be suggestive of Applicant's claim 1 limitations.

Thus, the cited combination of references does not show or suggest Applicant's claim 1 limitations.

5   For all of these reasons, a prima facie case of obviousness is not believed to have been established for this case, and this ground for rejection is traversed.

<u>Rejection of Claim 3 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of U.S. Patent No. 6,044,025</u>
10   <u>(*Lawman*).</u>

To the extent that this ground of rejection relies on the combination of *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the base claim limitations.

15   It is additionally noted that *Lawman*, like *Stroud et al.* and *Pathak et al.*, emphasizes testing via configuration data <u>stored in a tester</u>[7] – once again teaching away from Applicant's claim 1 limitations.

<u>Rejection of Claim 4 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*,</u>
20   <u>further in view of *Pathak et al.*, and even further in view of U.S. Patent No. 6,046,957 (*Shyu*).</u>

Claim 4, which depends from claim 1, recites that at least one nonvolatile store includes a first nonvolatile store formed with the programmable logic circuit on a single integrated circuit die.

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang*
25   *et al./Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the base claim limitations.

In addition, the references do not provide the suggestion/motivation to modify *Stroud et al./Kang et al./Pathak et al.* in view of *Shyu*, as proposed. As indicated above, the reference only
30   teaches self-test configuration data being included on a <u>tester</u>, or the like. The incorporation of

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[7] See *Lawman*, Col. 1, Lines 55-57

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tester functions into a system-on-a-chip (SOC) is beyond the suggested teachings of *Shyu*. In describing SOC trends, *Shyu* states the following:

5
> With the growing trend toward SOC (system-on-a-chip) technology, it is inevitable to incorporate a variety of <u>circuit building blocks</u>... onto a single integrated circuit chip... [A]n IP (intellectual property) based design approach is performed. The IP-based design approach involves the use of circuit building blocks having specific functions <u>that are well proven for the integration of the system chip.</u>[8]

10

Applicant asserts that a tester, as taught in *Stroud et al.* and *Kang et al.*, is not a circuit building block – and would not be considered obvious to include in an SOC.

Further, the rejection has not indicated how or if a nonvolatile store and programmable logic circuit are well proven for integration, as required by *Shyu*. Absent such a teaching, there is

15   not motivation modify the references as proposed. It is additionally noted that *Shyu* provides <u>no mention of programmable logic</u>, thus cannot provide the requisite suggestion/motivation for the proposed combination.

For all of these reasons, a prima facie case of obviousness has not been established for claim 4, and this ground for rejection is traversed.

20

<u>Rejection of Claims 5 and 6 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of U.S. Patent No. 4,771,399 (*Snowden et al.*).</u>

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang*

25   *et al./Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the limitations of base claim 1.

Further, to the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Pathak et al./Shyu*, the comments set forth above for claim 4 are incorporated by

30   reference herein. Namely, that the combination does not present a prima facie case of

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[8] *Shyu*, Col. 1, Lines 9-20, emphasis.

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obviousness for the limitations of base claim 4.

Rejection of Claims 7 and 8 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Cook,*
5 *Nigel P., A First Course in Digital Electronics, Prentice-Hall, 1999 pp. 684-689 (Cook).*

The rejection of claim 7 will first be addressed.

Claim 7, which depends from claim 4, recites that self-test configuration data on the at least one nonvolatile store is set by a manufacturing process step for a PLD assembly. Thus, the manufacturing step is directed to particular data: self-test configuration data.

10 The cited combination of references does not show such a limitation. In *Stroud et al.*, BIST configuration data is not set by, or related to, any manufacturing step for a PLD, as such data is maintained on a tester. *Kang et al.* is unrelated to self-test configuration data, and thus cannot be suggestive of Applicant's claim 7 limitation. *Pathak et al., Shyu,* and *Cook* provide no teachings regarding self-testing.

15 Accordingly, the combination of references cannot arrive at the limitations of claim 7.

Claim 8, which depends from claim 7, recites that at least one nonvolatile store includes a mask programmable read-only-memory (PROM) that stores self-test configuration data and a separate nonvolatile memory that can store user configuration data.

Applicant traverses the rejection of claim 8 based on a number of reasons.

20 First, the comments above for claim 7 are incorporated by reference herein.

Second, the references do not show or suggest the limitations of claim 8. Applicant's request clarification of how/where the combination of *Stroud et al./Kang et al./Pathak et al./Shyu/Cook* show the limitations of claim 8, as the references all teach single memories for configuration data, and not separate non-volatile memories.

25 Third, the rationale relied upon in rejecting claim 8 appears to be without basis. The rejection of claim 8 relies on the following reasoning.

[I]t would have been obvious for a person of ordinary skill in the art to provide a separate non-volatile memory that is programmable after manufacturing for
30 storing user configuration data... The motivation for doing so would be to allow the user to change the user-configuration of the programmable logic device after

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manufacturing, while leaving the self-test configuration data in the MROM since
it does not need to be changed after initial design prototyping of the
programmable logic device...[9]

5   Applicant's request clarification of where such a teaching is found in the cited references - as
Applicant has reviewed the reference in detail and has found no such teaching. The above
rationale appears to be a piecemeal reconstruction of the invention with the benefit of hindsight,
and thus is improper.

If it is being argued that the above modification to the references is well known (e.g.,
10   established by official notice), Applicant respectfully requests citation of a reference in support
of such action.

Rejection of Claims 9 and 10 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et
al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of
15   *Snowden*, yet further in view of U.S. Patent No. 5,668,816 *(Douskey et al.)*, and yet further in
view of U.S. Patent No. 5,032,533 *(Gill et al.)*.

Claim 9, which depends from claim 1, recites that at least one nonvolatile store includes
at least two sectors and self-test configuration data is stored in a first sector.

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang
20   et al./Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by
reference herein. Namely, that the combination does not present a prima facie case of
obviousness for the base claim limitations.

The rejection admits that the combination of *Stroud et al./Kang et al./Pathak et
al./Shyu/Snowden/Douskey et al.* does not show the limitations of claim 9[10]. To show such
25   limitations, the rejection relies on the following reasoning.

The motivation for making this modification [modifying *Stroud et al./Kang et
al./Pathak et al./Shyu/Snowden/Douskey et al.* in view of *Gill et al.*] would be to
simplify re-programming of a logic configuration by placing a single user

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[9] See the Office Action, dated 4/24/03, Page 9, Line 22 to Page 10, Line 2.
[10] See the Office Action, dated 4/24/03, Page 12, Lines 5-8.

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configuration in each flash memory block (i.e. sector). Thus, realizing the advantage of allowing one programmable logic configuration to be reprogrammed without affecting the other logic configuration.[11]

5 Applicant's request clarification of where this teaching can be found in the cited references - as Applicant has reviewed the references in detail and has found no such teaching. If it is being argued the above modification to the references is well known (e.g., established by official notice), Applicant respectfully requests citation of a reference in support of such a claim.

Still further, the above rationale cannot show or suggest why <u>self-test configuration data</u>
10 would be stored in one sector, as self-test data is not mentioned.

This ground for rejection is also traversed on the basis that there is no motivation to combine *Douskey et al.* with the combination *Stroud et al./Kang et al./Pathak et al./Shyu/Snowden.* *Stroud et al.* teaches the drawbacks of including BIST circuits in a device:

15   [A]dditional test... circuits increase complexity and space requirements...
        typically... between 10-30% and significant delay penalties in operating speed...[12]

In contravention to the explicit teachings of *Stroud et al.*, *Douskey et al.* purposely adds BIST circuits to an integrated circuit.[13] Thus, because the teachings of the reference teach against the
20 combination of *Douskey et al.* with *Stroud et al.*, motivation for the proposed combination is lacking and/or any prima facie case of obviousness has been rebutted.

For all of these reasons, this ground for rejection is traversed.

The rejections of claims 11-17 will now be addressed.

25

<u>Rejection of Claim 11 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden et al.*</u>

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[11] See the Office Action, dated 4/24/03, Page 13, Lines 6-11.
[12] *Stroud et al.*, Col. 1, Lines 34-40.
[13] See *Douskey et al.*, FIGURE 1, which shows BIST circuit 104 on the integrated circuit chip 100.

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Claim 11 has been amended to include limitations of claim 16. The invention of amended claim 11 is directed to a method that includes performing a self-test on a programmable logic circuit of one package according to self-test configuration data in a self-test nonvolatile store of the one package. The method also includes storing user configuration data in a user
5   nonvolatile store if the programmable logic circuit passes the self-test.

To address this ground of rejection, Applicant incorporates by reference the same general comments set forth for claims 1 and 2. Namely, just as the combination of *Stroud et al./Kang et al./Pathak et al.* does not show a programmable logic circuit and nonvolatile store of the same PLD assembly, the combination does not show a self-test on a programmable logic circuit
10 according to self-test configuration data in a self-test nonvolatile store, where the programmable logic circuit and self-test nonvolatile store are of the same package.

Accordingly, a prima facie case of obvious has not been established for this claim.

In addition, Applicant's reiterate comments set forth above for claim 9 and 10: *Stroud et al.* teaches the drawbacks of including BIST circuits in a device, which is in opposition to
15 *Douskey et al.*, which purposely adds BIST circuits to an integrated circuit. Thus, motivation for the proposed combination is lacking and/or any prima facie case of obviousness has been rebutted.

For all of these reasons, this ground for rejection is traversed.

20 <u>Rejection of Claims 12-15 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, still further in view of *Douskey et al.*</u>

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Shyu/Snowden*, the comments set forth above for claim 11 are incorporated by reference
25 herein. Namely, that the combination of references do not show all limitations of base claim 11.

In addition, with respect to claim 14, this claim recites storing user configuration data in locations that are different than those that store self-test configuration data. To address this rejection, Applicant incorporates the same general comments set forth above for claims 9 and 10. Namely, that rationale relied upon does not appear to be derived from the references.

30 With respect to claim 15, this claim recites forming a self-test nonvolatile store on the same die as the programmable logic circuit. To address this ground of rejection Applicant

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incorporates by reference herein the same general comments set forth above for claim 4.
Namely, that the reference do not show or suggest the limitations of claim 15.

Rejection of Claims 16 and 17 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang*
et al., further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of
Snowden, still further in view of *Douskey et al.*, in view of U.S. Patent No. 5,909,587 (*Tran*).

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang
et al./Shyu/Snowden*, the comments set forth above for claim 11 are incorporated by reference
herein. Namely, that the combination of references do not show all limitations of base claim 11.

In addition, this ground of rejection is traversed on a number of additional reason.

There is no motivation to add *Tran* to the above combination as the reference teaches
away from the express teachings of *Shyu*. The teachings of *Shyu* are directed to combining well
proven circuit blocks for integration into a single system chip (SOC). *Tran*, in express
contravention to the teachings of *Shyu*, is directed to separating functions into different chips.

Thus, because the *Tran* teaches away from the proposed modification, the requisite
suggestion/motivation for a prima facie case of obvious has not been established, or any prima
facie case of obviousness has been rebutted.

Rejection of Claims 18 and 19 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang
et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of
Snowden, still further in view of *Douskey et al.*

Claim 18 has been amended to include the limitations of claim 1. Amended claim 18 is
directed to a programmable logic assembly self-test method that includes the steps of: storing
self-test information in a first nonvolatile store of the assembly that places a programmable logic
circuit of the assembly into a self-test configuration; executing a self-test on the programmable
logic circuit; and providing user configuration information that places the programmable logic
circuit in a user configuration.

To address this ground for rejection the same general comments set forth above for
claims 1 and 2 are incorporated by reference herein. Namely, that the cited references are
directed to arrangements in which self-test is resident on a tester, not a nonvolatile store of an
assembly.

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<u>Rejection of Claim 20 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, still further in view of *Douskey et al.*, yet further in view of U.S. Patent No. 5,759,877 (*Crafts et*</u>

5   <u>al.)</u>

Claim 20, which depends from claim 18, includes user configuration data being stored in a second nonvolatile store that is different than the first nonvolatile store. The rejection of this claim relies on the following reasoning.

10   > The motivation for doing so [modifying *Stroud et al./Kang et al./Pathak et al./Shyu/Snowden/Douskey et al.* in view of *Crafts et al.*] would be to prevent the self-test data from being overwritten unintentionally by the user when user configuration data is programmed.[14]

15   Applicant's request clarification of where this teaching can be found in the cited references - as Applicant has reviewed the reference in detail and has found no such teaching. If it is being argued the above modification to the references is well known (e.g., established by official notice), Applicant respectfully requests citation of a reference in support.

Thus, because the rejection appears to rely on a teaching not set forth in cited reference, a

20   prima facie case of obviousness has not been established for this claim, and this ground for rejection is traversed.

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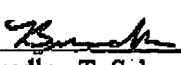
[14] See the Office Action, dated 4/24/03, Page 18, Lines 1-2.

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Claims 1-2, 7-8, 11, 14-16 and 18 have been amended. The present claims 1-20 are
believed to be in allowable form. It is respectfully requested that the application be forwarded
for allowance and issue.

5

Respectfully Submitted,

Bunch 7/22/03

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EXHIBIT A

Excerpts from

The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition

For Serial No.: 09/602,938
Applicant(s): MOORE, Michael

IEEE 100
The Authoritative Dictionary of
IEEE Standards Terms

Seventh Edition

channel   1113   store

top list.

g or wading pool A pool with
ft and a maximum wall height
at it may be readily disassembled
to its original integrity.

(electronic computation) The
(electronic computation) A
n can be stored, sometimes call
tronic computation) In a comp
ly for storing information usual
a memory or store (British) A p
f storing information may be ag
gnetic, acoustic, optical, or
echanical, etc., in nature. 2. A p
ata can be entered, in which
t can be retrieved at a later tim

ment) In a computer, one or
ore data.
tion of data in a storage devi
data into a storage device. (2)
edium in which data can b

access.

(1) (computers) The assign
instructions to specified object

element of computer resource
ning storage areas to specified
cedures, such as transfer of da
storage, to support the assign
uffer; contiguous allocation; re
clay; memory compaction.

'orage tubes) An assembly of
that contains the target togeth
trol of the storage process, the
nal, and other members used in
torage tube.   (BD)
ttery comprised of one or more
f-acid, nickel-cadmium, or oth
rl types.   (NES)
'se: data breakpoint.
low leakage capacitor on whi

The amount of data that can
Notes: 1. The units of capac
tc. For example, capacity
mal digits." "16 384-word st
rs each." 2. When comparing
ing different character sets,
nvenient to express the capa
the number obtained by taking
of the number of usable distin
torage can exist. 3. The short
mputer usually refers only to

maximum number of items
ge device; usually measured i
                         (C)
ata that can be contained in
binary characters, bytes, wor
                         (C)
ata that can be contained in
                         (BD)
ic energy) (secondary cell)
d for the generation of electri
being discharged, may be tra
ion by an electric current, the
the flow of current when

channel One or more storage elements considered as a unit.
smallest subdivision of storage into which a unit of
be placed, retained, and with which the unit can be
Synonym: data cell. See also: binary cell; magnetic
                         (C) 610.10-1994
ementary unit of storage (e.g., a binary cell or a
cell).   (BD/C) 1005-1998, [85], [20]
channel A channel that can be used to access a storage
                         (C) 610.10-1994w
vice (1) A device in which data can be stored and
which it can be copied at a later time. The means of
ata may be chemical, electrical, mechanical, etc. See
orage.   (C) 162-1963w
vice into which data can be placed, in which they can
ned, and from which they can be retrieved. See also:
                         (C) 610.10-1994w
isplay See: storage tube display device.
ficiency The degree to which a system or component
its designated functions with minimum consump-
available storage. See also: execution efficiency.
                         (C) 610.12-1990
lement (1) (storage tubes) An area of a storage sur-
at retains information distinguishable from that of ad-
areas. Note: The storage element may be a portion of
inuous storage surface or a discrete area such as a di-
island. See also: storage tube.
                         (BD) 158-1962w, 161-1971w
basic unit of a storage device, such as a sector, or a
                         (C) 610.10-1994w
ment equilibrium voltage (storage tubes) A lim-
storage toward which a storage element charges under
of primary electron bombardment and secondary
At equilibrium voltage the escape ratio is unity.
athode equilibrium voltage, second-crossover equilib-
voltage, and gradient-established equilibrium voltage
cal examples. See also: charge-storage tube.
                         (BD) 158-1962w
ement equilibrium voltage, cathode (storage tubes)
orage element equilibrium voltage near cathode voltage
low first-crossover voltage. See also: charge-storage
                         (BD) 158-1962w
ement equilibrium voltage, collector See: charge-
tube.
ement equilibrium voltage, gradient established
ge tubes) The storage-element equilibrium voltage, be-
first- and second-crossover voltages, at which the es-
ratio is unity. See also: charge-storage tube.
                         (BD) 158-1962w
ement equilibrium voltage, second-crossover (stor-
tubes) The storage-element equilibrium voltage at the
crossover voltage. See also: charge-storage tube.
                         (BD) 158-1962w
error An error in which the data retrieved from storage
erent from that which was originally stored in that lo-
See also: soft error; hard error; transient error.
                         (C) 610.10-1994w
(microprocessor operating systems parameter
An identifier for a block of data. The identifier is not
ited to be valid outside the allocating process and
not be passed between processes.
                         (C/MM) 855-1985s
integrator In an analog computer, a device used to store
age in the hold condition for future use. See also: elec-
analog computer.   (C) 610.10-1994w, 165-1977w
life (accelerometer) (gyros) (inertial sensors) The
operating time interval under specified conditions, after
h a device will still exhibit a specified operating life and
rmance. See also: operating life.
                         (AES/GYAC) 528-1994
light A light found on a storage device indicating that
rity check error has occurred on a character as it was read
                         (C) 610.10-1994w

storage light-amplifier See: image-storage panel.
storage location (1) An area in a storage device that can be
explicitly and uniquely specified by means of an address.
                         (C) 610.5-1990w
(2) A location in a storage device that is uniquely specified
by means of an address.   (C) 610.10-1994w
storage medium Any device or recording medium into which
data can be stored and held until some later time, and from
which the entire original data can be obtained.   (IA) [61]
storage protection (computers) An arrangement for preventing
access to storage for either reading or writing, or both.
                         (C) [20]
storage rate The frequency with which sampled signals are re-
corded in crashworthy nonvolatile memory. The event re-
corder may store any signal loss often than it samples.
                         (VT) 1482.1-1999
storage, reservoir See: reservoir storage.
storage schema In a CODASYL database, statements expressed
in data storage definition language that describe storage areas,
stored records, and any associated indices and access paths
supporting the records and sets defined by a given schema.
See also: CODASYL database.   (C) 610.5-1990w
storage stack See: stack.
storage station (power operations) A hydroelectric generating
station associated with a water storage reservoir.
                         (PE/PSE) 858-1987s, 346-1973w
storage structure (A) The manner in which data structures are
represented in storage. (B) The configuration of a database
resident on computer storage devices after mapping the data
elements of the logical structure of the database onto their
respective physical counterparts. Note: The relationships and
associations that provide the physical means for accessing the
information stored in the database are preserved.
                         (C) 610.5-1990
storage surface (storage tubes) The surface upon which infor-
mation is stored. See also: storage tube.   (BD) 158-1962w
storage temperature (1) (power supply) The range of envi-
ronmental temperatures in which a power supply can be
safely stored (for example, −40°C to +85°C).
                         (AES/IA) [41], [12]
(2) (light-emitting diodes) The temperature at which the de-
vice, without any power applied, is stored.   (ED) [127]
storage temperature range The range of temperatures over
which the Hall generators may be stored without any voltage
applied, or without exceeding a specified change in perform-
ance.   (MAG) 296-1969w
storage time See: decay time; maximum retention time.
storage tube An electron tube into which information can be
introduced and read at a later time. Note: The output may be
an electric signal and/or a visible image corresponding to the
stored information.   (BD) 161-1971w, 158-1962w
storage tube display device A type of cathode ray tube display
device that retains a display image on its surface in the form
of a pattern of electric charges. Synonyms: storage display;
display storage tube; direct-view storage tube. Contrast: re-
fresh display device.   (C) 610.10-1994w
storage unit The length of an addressable element of storage in
the machine, measured in bits. (Every storage element has the
same size.). Note: The storage unit is very likely to be one
byte, but this is not a requirement. For example, it might be
32 or 64 bits.   (C) 1003.5-1999
store (A) A device into which data can be placed, in which they
can be retained, and from which they can be retrieved. Note:
This term is the equivalent of the term storage in British
(U.K.) usage. (B) To place data into a device as in definition
(A). (C) To retain data in a device as in definition (A).
                         (C) 162-1963, 610.10-1994
(2) (A) To place or retain data in a storage device.
(B) (software) (data management) To copy computer in-
structions or data from a register to internal storage or from
internal storage to external storage. Contrast: retrieve; load.
See also: move; fetch.   (C) 610.12-1990, 610.5-1990